

WHAT IS CLAIMED IS:

1           1.    A filter circuit comprising:  
2                a first differential transistor pair biased by a first  
3                differential input;  
4                a second differential transistor pair biased by a second  
5                differential input, the second input having been received  
6                prior to the first differential input;  
7                at least one current source coupled to provide tail  
8                currents for the differential pairs;  
9                wherein the transistors which are biased by present and  
10               previous inverted inputs have a first output terminal; and  
11               wherein the transistors which are biased by present and  
12               previous non-inverted inputs have a second output terminal.

1           2.    The filter circuit of claim 1, wherein the output  
2                nodes are coupled to at least one load selected from the group  
3                consisting of a regenerative latch, a passive load, an active  
4                filter, and an amplifier.

1           3.    The filter circuit of claim 1, wherein the tail  
2                current of the first differential pair is different than the  
3                tail current of the second differential pair.

1           4.    The filter circuit of claim 3, wherein the tail  
2   currents are provided by a plurality of variably controlled  
3   current sources.

1           5.    The filter circuit of claim 3, wherein the tail  
2   current differential is provided by a difference in channel  
3   widths between the first and second transistor pairs.

1           6.    The filter circuit of claim 1, further comprising  
2   first and second offset-inducing differential pairs connected  
3   in parallel to the first and second differential pairs,  
4   respectively.

1           7.    The filter circuit of claim 6, wherein the channel  
2   widths of the transistors in each differential pair are not  
3   equal and wherein the difference in channel width in the  
4   offset-inducing differential pairs is opposite that of the  
5   first and second differential pairs.

1           8.    The filter circuit of claim 7, wherein the tail  
2   currents for the first and second offset-inducing differential  
3   pairs are equally and oppositely offset from a nominal current  
4   level relative to the tail current for the first or second  
5   differential pairs, respectively.

1           9.    The amplifier circuit of claim 8, wherein the output  
2   nodes provide an amplified, offset and filtered differential  
3   signal.

1           10.   The filter circuit of claim 1, wherein the  
2   transistors of the differential pairs are p-channel MOSFET  
3   transistors.

1           11.   The filter circuit of claim 1, wherein the output  
2   nodes provide an amplified, offset and filtered differential  
3   signal.

1           12.   The filter circuit of claim 1, further comprising a  
2   third differential pair being biased by a third differential  
3   input received after the first differential input, the  
4   transistor which is biased by an inverted input being coupled  
5   to the first output node and the transistor which is biased by  
6   a non-inverted input being coupled to the second output node.

1           13.   The filter circuit of claim 1, wherein the output  
2   nodes are connected to an input of another circuit element.

1        14. A filtering method comprising:  
2        receiving first and second differential inputs, the  
3        second input having been received prior to the first input;  
4        biasing the first and second differential input pairs  
5        with the first and second differential inputs, respectively;  
6        weighting the first and second differential inputs by  
7        modulating the gain of at least one of the differential input  
8        pairs;  
9        tapping the first and second output nodes to obtain a  
10       filtered signal, wherein the first and second output nodes are  
11       connected to the transistors which are biased by the inverted  
12       inputs and non-inverted inputs, respectively.

1        15. The method of claim 14, wherein the output nodes are  
2        coupled to at least one load selected from the group  
3        consisting of a regenerative latch, a passive load, an active  
4        filter, and an amplifier.

1        16. The method of claim 14, wherein the gain is  
2        modulated by altering the tail currents of the differential  
3        pairs.

1           17. The method of claim 14, wherein the gain is  
2 modulated by altering the tail currents provided by a  
3 plurality of variably controlled current sources.

1           18. The method of claim 14, wherein the gain is  
2 modulated by altering the widths of the channels of the  
3 transistors.

1           19. The method of claim 14, further comprising inducing  
2 an offset by connecting first and second offset-inducing  
3 differential pairs in parallel to the first and second  
4 differential pairs, wherein the channel widths in at least one  
5 transistor pair are mismatched.

1           20. The method of claim 19, further comprising inducing  
2 an offset in a third differential input, the third  
3 differential input having been received after the first  
4 signal.

1           21. The method of claim 19, further comprising equally  
2 and oppositely offsetting the tail currents of the first and  
3 second offset-inducing differential pairs from a nominal  
4 current level relative to the tail current for the first or  
5 second differential pairs, respectively.

1           22. The method circuit of claim 14, wherein the filtered  
2 signal is also amplified and offset.

1           23. The method of claim 14, wherein the transistors of  
2 the differential pairs are n-channel MOSFET transistors.

1           24. The method of claim 14, further comprising receiving  
2 a third differential signal, the third signal having been  
3 received after the first signal, biasing a differential input  
4 pair with the third signal, and weighting the third signal by  
5 modulating the gain of at least one of the differential input  
6 pairs.

1           25. A communications system comprising:

2           (a) a transmitter producing a differential voltage  
3 signal;

4           (b) a receiver comprising:

5               (1) a sample-and-hold circuit that receives the  
6 differential voltage signal and samples and holds values  
7 of the differential voltage signal; and

8               (2) a filter circuit comprising:

9                   a first differential transistor pair  
10                   biased by a first differential input;

11 a second differential transistor pair  
12 biased by a second differential input, the  
13 second input having been received prior to the  
14 first differential input;

15 at least one current source coupled to  
16 provide tail currents for the differential  
17 pairs;

18 wherein the transistors which are biased  
19 by present and previous inverted inputs have a  
20 first output terminal; and

21 wherein the transistors which are biased  
22 by present and previous non-inverted inputs  
23 have a second output terminal.

1 26. The communications system of claim 25, wherein the  
2 transmitter and the receiver reside on different circuit  
3 boards.

1 27. The communications system of claim 25, wherein the  
2 transmitter and the receiver reside on different integrated  
3 circuit die.

1 28. The communications system of claim 25, wherein the  
2 filter further comprises first and second offset-inducing

3 differential pairs connected in parallel to the first and  
4 second differential pairs, respectively, wherein the channel  
5 widths of the transistors in each differential pair are not  
6 equal and wherein the difference in channel width in the  
7 offset-inducing differential pairs is opposite that of the  
8 first and second differential pairs.